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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/628,594	07/28/2003	Robert C. Sundahl	884.264US2	4636

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SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER	
NGUYEN, DONGHAI D	

ART UNIT	PAPER NUMBER
3729	

DATE MAILED: 06/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

c

Office Action Summary	Application No.	Applicant(s)	
	10/628,594	SUNDAHL ET AL.	
	Examiner	Art Unit	
	Donghai D. Nguyen	3729	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13 and 23-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13 and 23-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment filed on April 13, 2006 has been considered and made of record.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 23-27 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent 5,801,446 to DiStefano et al.

Regarding claim 23, DiStefano et al disclose a method comprising: placing at least one spacer (30/134) on at least one first bond pad (26/126) of a first circuit board (chip mounting substrate, circuit panel, or circuit board 25 or 102) such that the spacer directly contacts the first bond pad (see Col. 11, lines 11-13), wherein the spacer is formed of a conductive material (Cu, Ni, etc.,) that remains in a solid form (Col. 6, lines 40-42) during attachment of the first circuit board to a second circuit board (50/150); aligning the first circuit board (25/102) with the second circuit board (50/150) by engaging the spacer (30/134) with an opening (see Figs. 1-5) in the second circuit board so that a second bond pad (52/152) of the second circuit board aligns with

the first bond pad, and the spacer directly contacts the second bond pad (see Col. 11, lines 11-13); and attaching the first circuit board to the second circuit board (see Fig. 1-3.

Regarding claims 24 and 25, DiStefano et al disclose applying a conductive material (solder see Col. 11, lines 13-16) in proximity to an area of the spacer and the first bond pad before attaching the first circuit board to the second circuit board and heating the conductive material to allow the conductive material to directly contact the first bond pad and the second bond pad (Col. 11, lines 16-19).

Regarding claims 26 and 27, DiStefano et al disclose inserting an insulating material (42, 151 or 136) in an interface region between the first circuit board and the second circuit board wherein, the insulating material to only one of the first circuit board and the second circuit board before attaching the first circuit board to the second circuit board (see Figs. 1-5).

4. Claims 23-27 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent 6,324,754 to DiStefano et al.

Regarding claim 23, DiStefano et al disclose a method comprising: placing at least one spacer (42) on at least one first bond pad (20) of a first circuit board (chip mounting substrate, circuit panel 16) such that the spacer directly contacts the first bond pad (see Fig. 3), wherein the spacer is formed of a conductive material (Cu) that remains in a solid form (Figs. 3-4 and Col. 7, lines 58-65) during attachment of the first circuit board to a second circuit board (10); aligning the first circuit board (16) with the second circuit board (10) by engaging the spacer (42) with an opening (see Fig. 4) in the second circuit board so that a second bond pad (52) of the second

circuit board aligns with the first bond pad, and the spacer directly contacts the second bond pad (see Fig. 4); and attaching the first circuit board to the second circuit board (see Fig. 5-6).

Regarding claims 24 and 25, DiStefano et al disclose applying a conductive material (flux see Col. 7, lines 35-44) in proximity to an area of the spacer and the first bond pad before attaching the first circuit board to the second circuit board and heating the conductive material to allow the conductive material to directly contact the first bond pad and the second bond pad (Col. 7, lines 53-56).

Regarding claims 26 and 27, DiStefano et al disclose inserting an insulating material (32) in an interface region between the first circuit board and the second circuit board wherein, the insulating material to only one of the first circuit board and the second circuit board before attaching the first circuit board to the second circuit board (see Figs. 1-4).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-9 and 30-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over either DiStefano et al (as applied to claim 23 above) in view of US Patent 5,703,394 to Wei et al.

Regarding claims 1 and 4, both DiStefano et al references disclose all the limitations that recited in claim 1 (see rejection of claim 23 above) except that the second circuit board having multiple optoelectrical display elements which electrically connected to one or more second

bonding pads. However, Wei et al teach the circuit board (12) having multiple optoelectrical display elements (11) which electrically connected to one or more bonding pads (16) for forming an organic light emitting device (see Figs. 1-2). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the inventions of DiStefano et al by providing the teaching fabricating the circuit board having multiple optoelectrical display elements that electrically connected to one or more bonding pads as taught by Wei et al as to form the organic light emitting device for manufacturing the interconnected circuit board assembly.

Regarding claims 2 and 3, both DiStefano et al references do not teach the forming spacers by electroplating and welding the spacers to the bonding pads. Regarding the limitation as described above it would have been an obvious matter of design choice to form at least one the spacer by electroplating process and further to connect/attach the at least one spacer to the bonding pads by welding, since Applicants have not disclosed that the above forming the spacers by electroplating process and attaching the spacers to the bonding pads by welding is critical and patentable method features that would solve any stated problem or is for any particular purpose and it appears the invention would perform equally well with the teaching as taught by DiStefano et al reference (i.e. see discussion at Col. 11, lines 3-35)

Regarding claims 5-9, DiStefano et al (reference '446) disclose the applying a conductive material (solder 34 or 132 and Col. 11, lines 8-11) in proximity of the spacers (Figs. 1-5) or in contact with each of the one or more spacers and heating the conductive (Col. 7, lines 26-33). DiStefano et al (reference '754) also disclose the applying a conductive material (solder or solder

flux and Col. 7, lines 35-44) in proximity of the spacers (Figs. 3-4) or in contact with each of the one or more spacers and heating the conductive (Col. 7, lines 53-56).

The limitations of claims 30 and 31 also met as detail in the rejection of claim 1 above.

7. Claims 10-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over either one of DiStefano et al in view of Wei et al as applied above, and further in view of Marrs.

Both DiStefano/Wei et al as applied and relied above do not disclose the process of injecting an insulated material in an interface region between the first and second circuit boards. Marrs teaches the injecting the insulating material (901,199 and/or 601) into the interface region (Col. 10, lines 47-65) between the first and second circuit boards (201/501) or inserting the insulating material to one of the circuit prior to attaching the first circuit board to the second circuit board and curing the insulating material (Fig. 7-8) then fully cure the insulating material for protecting the connection from the ambient environment (Col. 10, lines 49-54). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of DiStefano/Wei et al by incorporating the Marrs' teachings as described above in order to facilitate the fabrication process including protecting the connections from the environment.

8. Claims 28-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over either one of DiStefano et al in view of US Patent 5,795,818 to Marrs.

Regarding claims 28 and 29, DiStefano et al do not disclose the injecting the insulating material into the interface region that isolating the insulating material from the first bond pad and the second bond pad. Marrs teaches the injecting the insulating material (901,199 and/or 601) into the interface region (Col. 10, lines 47-65) between the first and second circuit boards (201/501) for protecting the connection from the ambient environment (Col. 10, lines 49-54). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the inventions of DiStefano et al by incorporating the Marrs' teachings as described above in order to facilitate the fabrication process including protecting the connections from the environment.

Response to Arguments

9. Applicants' arguments with respect to claims 1-13 and newly added claims 23-31 have been considered but are moot in view of the new ground(s) of rejection.

10. Applicants' arguments filed April 13, 2006 have been fully considered but they are not persuasive. Applicants argue that DiStefano et al do not disclose the spacer(s) directly contacting the second bonding pad(s) (see "Remarks" page 7). The Examiner disagrees because DiStefano et al reference '446 disclose the spacer(s) directly contacting the second bonding pad(s) (see Col. 11, lines 11-13).

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donghai D. Nguyen whose telephone number is (571)-272-4566. The examiner can normally be reached on Monday-Friday (9:00-6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Peter D. Vo can be reached on (571)-272-4690. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DN

June 12, 2006

MINH TRINH
PRIMARY EXAMINER